REMARKS

Claims 1-3, 6-19, and 22-40 were examined and reported in the Office Action dated May 12, 2004. Claims 1-3, 6-19, and 22-40 were rejected. Claims 1, 10, 17, 24, 29 and 36 are amended. Claims 1-3, 6-19, and 22-40 remain.

Applicant requests reconsideration of the application in view of the following remarks.

It is asserted in the Advisory Action that the claims will not be entered because the amended claims are not enabled in the specification and that "[t] specification fails to show that each sub-PLA of the plurality of sub-PLAs has an OR plane." Also, the box on PTOL-303 is checked for raising an issue of new matter. Applicant respectfully traverses the aforementioned reasons for not entering the claims for the following reasons. On page 4 of Applicant's original specification it is asserted that "[a] PLA is merely a set of two-level logic functions in n boolean input variables. By two-level logic, we mean AND and **OR**." Applicant asserts that one of ordinary skill in the art would know that PLAs, and thus sub-PLAs, contain both AND and OR planes. All sub-PLAs have an AND and an OR plane . See also the specification page 6, line 18 et al. describing splitting a PLA into sub-PLAs, which each have and AND and an OR plane.

Further, on page 8 of Applicant's specification, it is asserted that "[t]he embodiment presented above in Figure 2 thus **has an extended OR plane** resulting from interleaving **the OR planes of the two sub-PLAs**." Page 10 of the original specification asserts that "[o]ne skilled in the art will note that the AND plane is identical to the embodiment illustrated in Figure 2, including the NAND gates interposed between the AND and **OR planes**." And, page 12 of the original specification asserts "[I]t should be noted that there are some small changes to the logic between the AND and **OR planes**." (discussing sub-PLA-a and sub-PLA-b).

Therefore, no new matter was added in the response filed on June 2, 2004 and the original specification is enabling as to the limitation "each sub-PLA of the plurality of

sub-PLAs has an OR plane" as each sub-PLA (and each PLA) has an AND plane and an OR plane, which was fully described in the original specification and is known to one of ordinary skill in the art of programmable logic arrays.

CONCLUSION

In view of the previously submitted response and the foregoing, it is submitted that claims 1-3, 6-19, and 22-40 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

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Dated: July 16, 2004

By: _____
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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on July 16, 2004.

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Jean Svoboda